Academic Year 2014-15

Annexure I

1. Project Title: Design of multi gigabit links on high density PCB inter connects and optimization of via-stubs

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1. Abstract & Objective

1.1 Abstract

In olden days of 10MHz clock frequencies, the chief design challenges of printed circuit boards (PCB's) and packages were how to route signals on a simple two layer printed circuit board and how to get packages that wouldn't crack during assembly. The electrical properties like rise time, impedance discontinuities, quarter wave stubs have no effect in degrading the performance of the system at that frequencies.

But in current modern applications like Giga-bit & Tera-bit routers, DDR3 & DDR4 SD-RAM memories, 3G-4G or LTE-A base stations, broad band applications etc., the clock frequencies are running in hundreds of MHz and GHz range. So the interconnects used between the transmitter and receiver are no more transparent and the impedance discontinuities start reflecting the signals. Even the frequency dependent losses like copper loss and dielectric loss have much more impact at these frequencies. Further the non-linear effects like surface roughness (Cu Rz) and glass weave effect of di-electric, effect the performance of inter-connects and result in low bit error rate. The decrease in the rise time's of the signals in real time application's has become a challenge for signal integrity engineer's for ensuring proper eye opening and to meet timing at receivers. Especially timing margins have become so burdensome for applications which use DDR3 (or 4) SD-RAMS.

As a result of high band width applications in real time, there is a requirement of High Density Interconnect (HDI) board's which involve more than 24 layers of PCB stack-up. Requirements demand minimum spacing between inter-connects which increase cross-talk between signals resulting in failure of signal integrity at receiver. Further, complex via structure's in the inter-connect through which signal can be guided to the internal layers of stack-up appear as capacitive discontinuities which results in high reflection loss. In recent days much technical advancement happened in PCB fabrication units where the stub's on via can be removed using back-drilling. Advancement in via design extended upto the micro-via, blind-via and buried-via. By using these technologies, via can be designed transparently so that it doesn't appear as impedance discontinuity.

The objective of this project is to design a transparent interconnect on a 20 layer PCB stack-up with a 100 Ohm differential impedance with six inter-connects on the board. The differential spacing between inter-connects has to be maintained so that differential cross-talk is minimum. The

transmitter and receiver are modelled as Input Buffer Information Specific (IBIS) models where the models has V-I characteristics information of particular buffer. Further the inter-connect via structures will be optimized so that channel performance will be better. S-parameter analysis will be done so to observe the channel performance in frequency domain. Eye diagram and bath tub curve analysis will be performed to see the BER plots. TDR analysis will be performed to view the impedance w.r.t propagation delay of channel through which impedance of discontinuities can be debugged and corrected.

1.2 Motivation

Now a days we have been seeing the lot of waiting and traffic at toll plaza due to manual collection of money. This process kills valuable time and also wastage of fuel due to slow and stopping movement of vehicles at the toll plaza. This process motivated to design a automatic system to overcome this problems of waiting and fuel consumption at toll plaza. It can be useful to identify theft vehicles also

Main aim of our project:

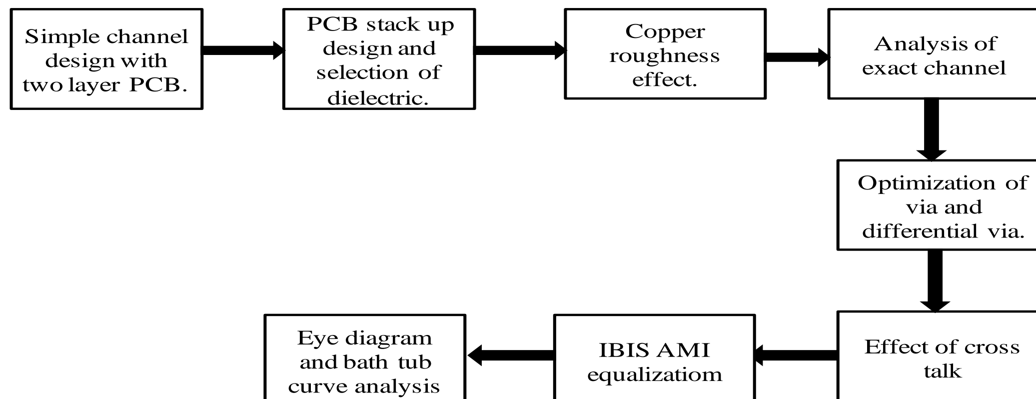
1. Save the time
2. Avoid the fuel loss
3. Identify theft vehicles
4. To avoid traffic

1.3 Objective

The objective of this project is to design a transparent interconnect on a 20 layer PCB stack-up with a 100 Ohm differential impedance with six inter-connects on the board. The differential spacing between inter-connects has to be maintained so that differential cross-talk is minimum. The transmitter and receiver are modelled as Input Buffer Information Specific (IBIS) models where the models has V-I characteristics information of particular buffer. Further the inter-connect via structures will be optimized so that channel performance will be better. S-parameter analysis will be done so to observe the channel performance in frequency domain. Eye diagram and bath tub curve analysis will be performed to see the BER plots. TDR analysis will be performed to view the impedance w.r.t propagation delay of channel through which impedance of discontinuities can be debugged and corrected.

2. Block Diagram & Technical Specifications

2.1 Block Diagram and Working:



2.1.2. Description:

A simple channel will be designed with two layer PCB board and it is interconnected on PCB stack up. The dielectric material is selected and copper roughness effect will be analysed with exact channel. The optimization of via and differential via configurations will be analysed and effect of cross talk will be examined. The transmitter and receiver are modeled as Input Buffer Information Specific (IBIS) where the models has V-I characteristic information of particular buffer. S-parameter analysis will be done to observe channel performance in frequency domain. At the end, Eye diagram and bath tub analysis will be performed to see the BER plots.

2.1.2.1 Simple Channel Design with two layer PCB:

This block of project will be the fundamental inorder to design the PCB stack up. In this block, a simple PCB stack up will be designed, so to achieve controlled impedance by considering different combinations of micro strip lines and strip lines.

2.1.2. 2 PCB stack-up design and selection of dielectric material:

In this block of project, selection of dielectric material and PCB stack up are the important targets. Wide varieties of dielectric material are available in market. Among them multiple simulations will be performed to analyze the performance of each dielectric material. Considering the dielectric loss the best material will

be chosen and accordingly PCB stack-up will also be developed by combining different laminates/ Prepregs and cores

2.1.2. 3 Copper Roughness effect

Copper roughness plays an important role in determining the copper loss of the foils used. As this has direct effect on the insertion loss care must be taken to choose the smooth copper. Further analysis will be done for finding the acceptable amount of roughness.

2.1.2. 4 Analysis of exact channel

Finally, after designing the channel will the above mentioned blocks, eye diagram analysis and S-parameter analysis will be done for finding the performance of the channel designed. Channel will be improved accordingly based on the performance and some optimization should be done for meeting the design requirements.

2.1.2.5 Optimization of Differential Via

Via should be designed with care, as the impedance discontinuity will have significant effect on the return loss directly and channel may give worst performance if via design is worst. So, using Time Domain Reflectometer (TDR) and S-parameters (Return loss) via will be optimised that channel performance meets the requirements.

2.1.2.6 Cross Talk and IBIS AMI equalization

Cross talk from aggressors can change the rise times and close the eye opening in the eye diagram. So, using S-parameter analysis trace to trace separation can be found out so that cross talk effects are minimum.Equalization techniques are used at the receiver so that even channel is worse receiver will be able to decode the data sent from transmitter.

2.1.2. 7Eye Diagram analysis and bath tub curves

BER will be measured from the bath tub curves and for low BER's channel will be improved and using equalization techniques the data will be reconstructed again. Eye diagram analysis will be performed to measure the eye height for meeting sensitivity of receiver and eye width for meeting the set-up and hold time requirements at the receiver.Finally the goal of the project is to design a transparent channel for meeting the receiver specifications.

2.2 Technical specifications:

Advanced Design System (ADS) continues to lead the RF EDA industry with the most innovative and commercially successful technologies, including Harmonic Balance, Circuit Envelope, Transient Convolution, Keysight Ptolemy, X-parameter*, Momentum and 3D EM simulators (including both FEM and FDTD solvers). With ADS's Wireless Libraries and circuit-system-EM co-simulation technology, ADS provides full, standards-based design and verification within a single, integrated platform.

Advanced Design System (ADS) is the flagship product from Keysight EEsof EDA, the technology and innovation leader in high-frequency, mixed-signal electronic design automation (EDA). It is the only design simulation platform that enables the co-design of IC, package and board in high-frequency and hi-speed applications. ADS seamlessly integrates system, circuit, and full 3D electromagnetic simulation with Keysight's test instrumentation to perform single pass successful electronic designs repeatedly.

Previously sold separately, the combined capabilities in ADS Core assure you the best value in RF design capabilities available anywhere. For example, design guides automate the synthesis of filter and multi-stage matching networks to reduce hours of designs to minutes. The high quality of software engineering behind ADS provides a stable platform for the creation, sharing and management of your valuable intellectual properties.

From ADS Core, you can add other circuit, system and electromagnetic simulation capabilities to complete even the most challenging designs. Your careful choice of ADS Core represents joining a growing installed base of over 12,000 successful designers worldwide.

The Advanced Design System (ADS) **Design Environment** is the graphical user interface for schematic entry and simulation setup within the W2200 ADS Core.All schematic RF, system and digital signal processing (DSP) designs are captured within the Design Environment including the configuration of simulation and optimization, setting variables, viewing libraries, and running DesignGuides.The Design Environment provides the integration and design capture framework for plugging in other ADS modules, including simulators, layout, and models, libraries and DesignGuides.

2.3 Results

2.3.1 Case A- S-parameter simulation for whole channel with Circular anti-pad (NFPs Not removed) Differential Via

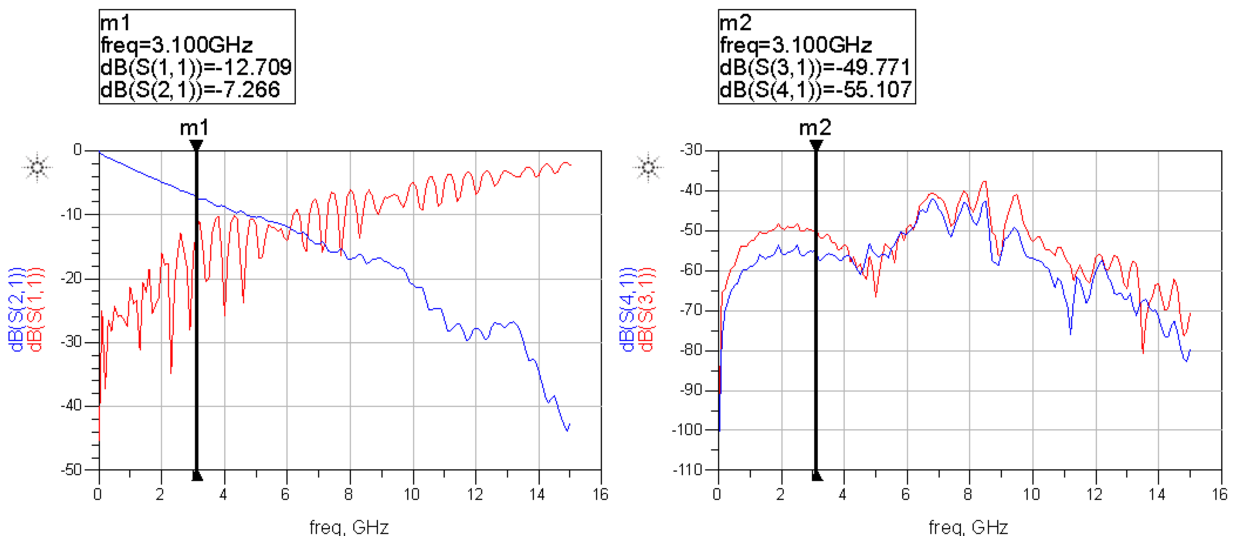


Figure 1: S-parameter simulation for whole channel with Circular anti-pad (NFPs Not removed) Differential Via

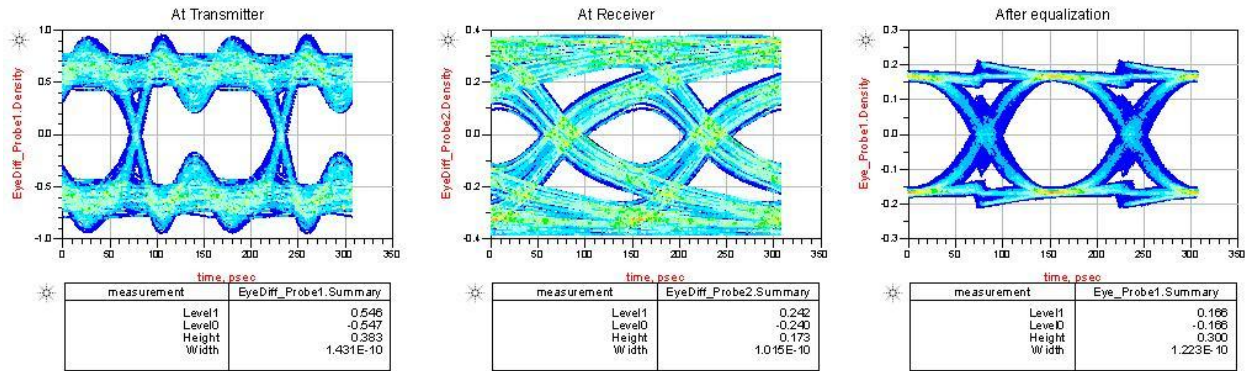


Figure 2: Eye diagram for whole channel with Circular anti-pad (NFPs Not removed) Differential Via

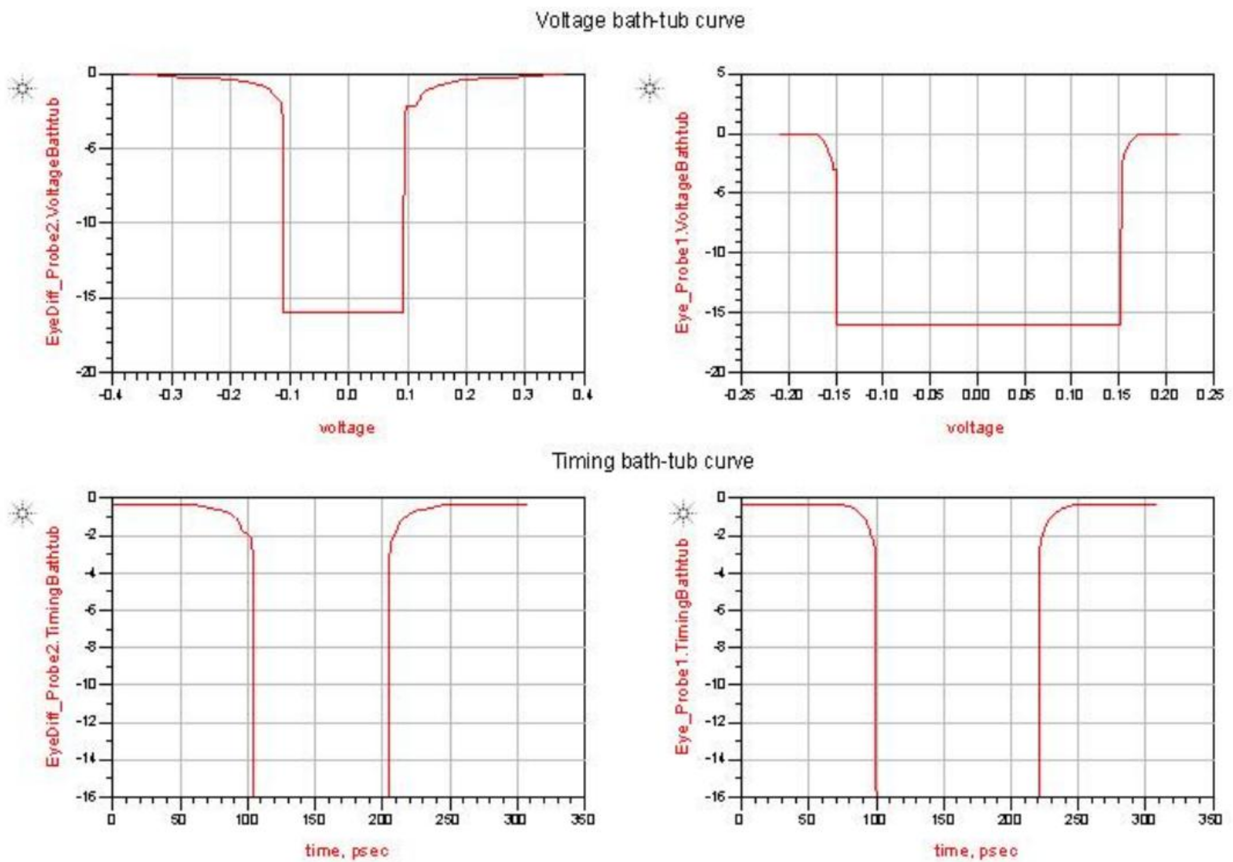


Figure 3: Bath-tub curve for whole channel with Circular anti-pad (NFPs Not removed) Differential Via

2.3.2 Case B- S-parameter simulation for whole channel with Circular anti-pad Via

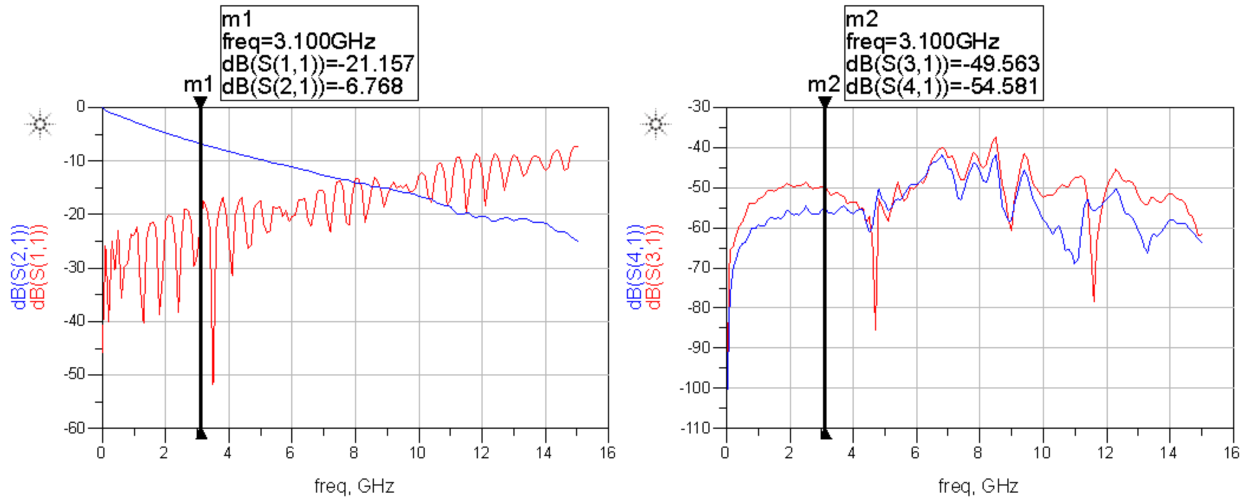


Figure 4: S-parameter simulation for whole channel with Circular anti-pad Via

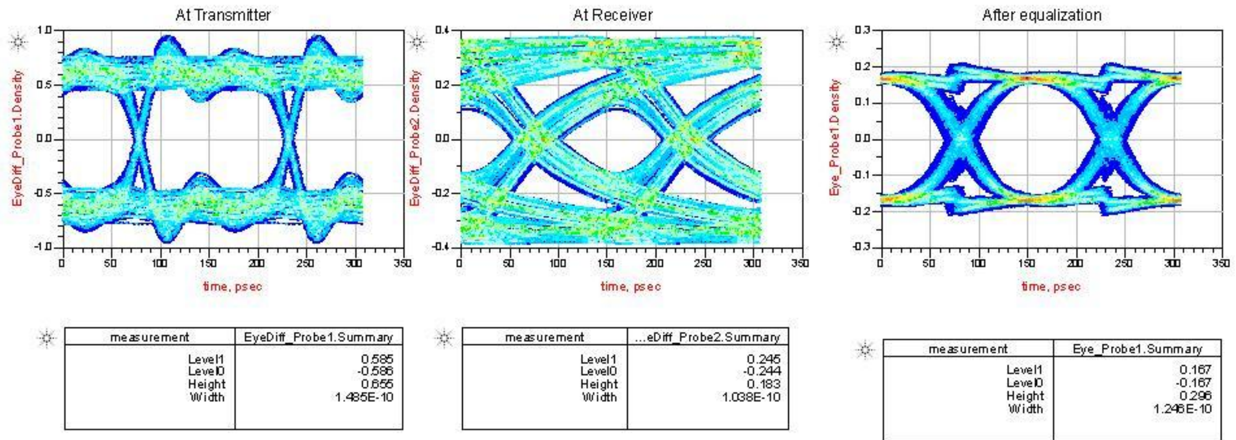


Figure 5: Eye diagram for whole channel with Circular anti-pad Via

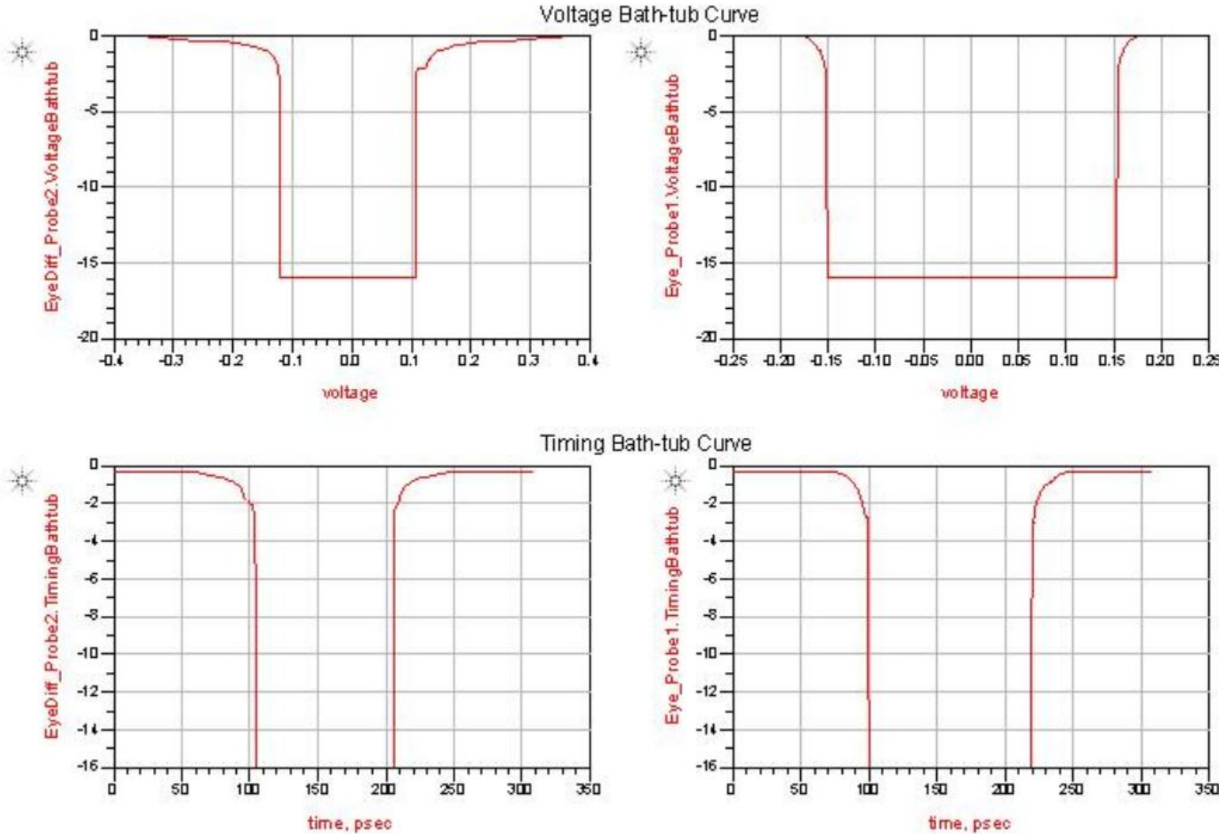


Figure 6: Bath tub curve for whole channel with Circular anti-pad Via

2.3.3 Case C- S-parameter simulation for whole channel optimized Differential Via

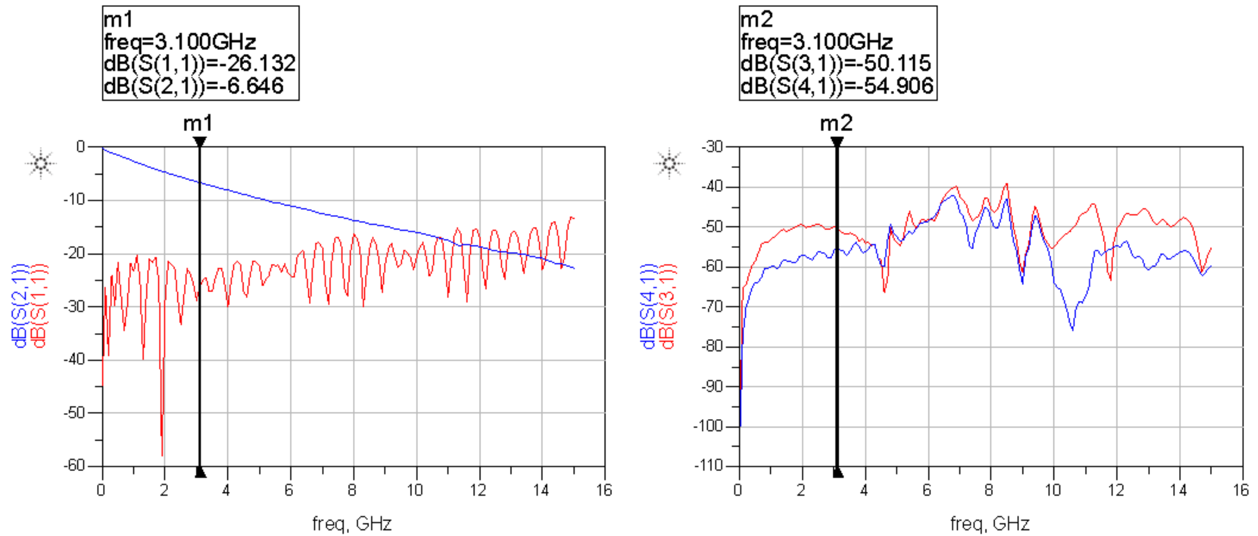


Figure 7: S-parameter simulation for whole channel optimized Differential Via

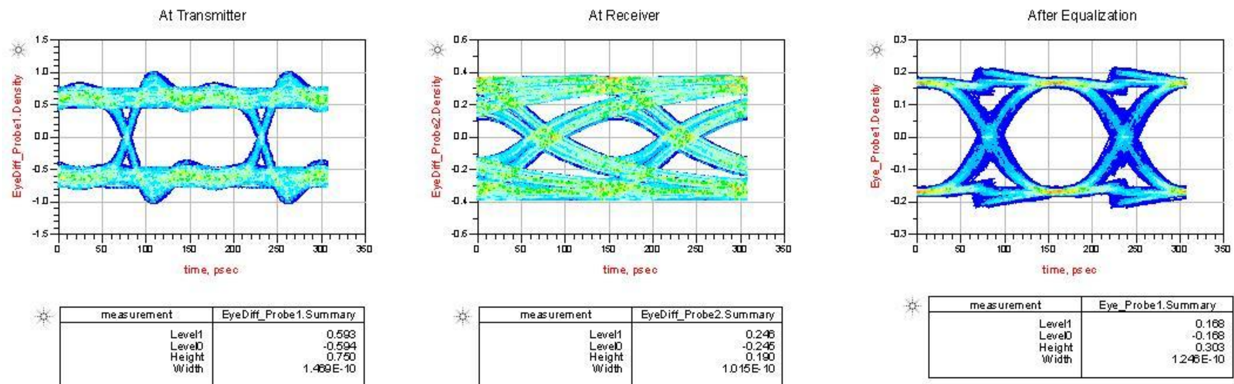


Figure 8: Eye diagram for whole channel optimized Differential Via

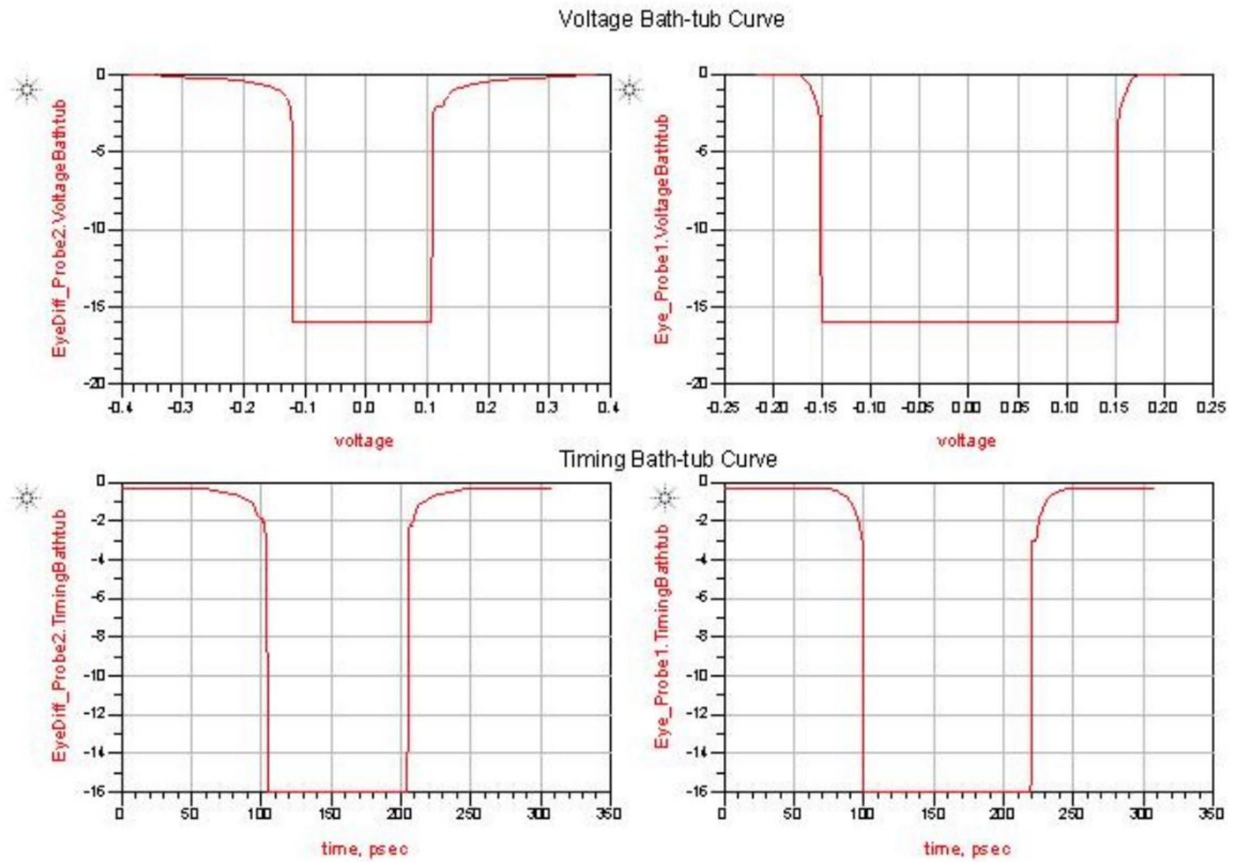


Figure 9: Bath tub curve for whole channel optimized Differential Via

2.4 Consolidated results and Conclusion

Case	Insertion Loss(dB)	Return Loss(dB)
A	-7.266	-12.709
B	-6.768	-21.157
C	-6.646	-26.132

Case	Near End X-talk(dB)	Far End X-talk(dB)
A	-49.771	-55.107
B	-49.563	-54.581
C	-50.115	-54.906

Cross talk really did not change much as the setting for spacing in three simulations did not change and is meeting the specification. But there is a severe problem when it comes to return loss. Return loss is very high in case A and the best value is given by case C. So, via optimization is really improving the return loss and helping in meeting the specification

Case	After Channel		After Equalization	
	Eye Height(mV)	Eye Width(ps)	Eye Height(mV)	Eye Width(ps)
A	173	101.5	300	122.3
B	183	103.8	296	124.6
C	190	101.5	303	124.6

After channel results shows the significant improvement in eye height as the channel is optimized. However there is no much improvement in width. After equalization results show that even if channel is bad it can be improved by equalization and both eye height and width are improved in three cases.But Best channel is case C.

3. Conclusion

3.0. Conclusion

Hence the transparent channel is well designed, improved and optimized using various techniques in order to meet the specifications.